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Re: Form No. GA26-3645-5

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Previous Newsletter Nos. None

This Technical Newsletter provides replacement pages for the IBM 1130 Computing System Storage Access Channel Original Equipment Manufacturers' Information, Form A26-3645. Pages to be inserted and/or removed are listed below.

21-22
25-26
49-50

A change to the text or a small change to an illustration is indicated by a vertical line to the left of the change; a changed or added illustration is denoted by the symbol (●) to the left of the caption.

Summary of Amendments:

1. Correction to timing information concerning loading of SBR during sense operation.
2. Correction of twist statement for bulk cable to OEM device.
3. Changes to I/O signal panel (Figure 33) drawing noting need for specific connectors.

File this cover letter at the back of the manual to provide a record of changes.

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On a Sense instruction the SBR is loaded at T1. Some SAC II users may not get channel write gate up in time. In such cases channel write gate and the sense data should be brought up during the E-1 cycle; but also be aware of the exposure in Example 1 below.

3. XIO Read Operation. The channel write gate should be made active so as to provide the data into the SBR during the CPU time interval E3-T2 to E3-T4.

Note: Since the channel write gate is used for data transfer into the SBR, circuits must be provided to insure that data in the SBR is not destroyed if two SAC operations try to overlap. The preceding procedures (1, 2, and 3) must be followed in designing the user's attachment to insure data integrity.

Two hypothetical examples are given next to illustrate the possible misuse of the channel write gate.

Example 1.

Assume that the SAC is transferring data to the CPU using interrupt operation (direct program control, either the XIO Read or an XIO Sense command). Also assume that the channel write gate is activated, by a SAC device, during the E-1 cycle. Suppose that, because of a previous XIO Initiate Write command, the SAC steals the next cycle to transfer data from core storage. Now, since the channel write gate is active (for the Read or Sense) and the SAC recognizes its cycle-steal, the interrupting data will be loaded into the SBR, by mistake, at X3 time of the cycle-steal, thus destroying the cycle-steal data.

The XIO Sense command example is illustrated in Figure 12.

Example 2.

Assume that a system device (not requiring channel write gate) is interrupting sense data into core storage, and that a SAC cycle-steal request comes up just after E2-T0. Suppose that the SAC user's device activates the channel write gate at this time. Now, since the channel write gate is active, whatever is on the data in bus is loaded into the SBR along with the data from the system device that was interrupting, thus destroying the desired data. The same condition could exist for read data, but during the E-3 cycle instead of the E-2 cycle.

Block Clock Advance: This line may be used by the SAC to inhibit advance of the cycle-steal clock during a channel cycle-steal operation. The cycle-steal clock can be stopped only at X2 or X7. Care must be used to prevent blocking the cycle-steal clock while another device is also cycle-stealing, because data from or to that device may be lost. Also, if the X-clock is stopped at X2, the same address must be used for the completion of the cycle.

To stop the cycle-steal clock at X2, block clock advance must be at the CPU terminator no sooner than X0 and no later than the leading edge of X2.

To stop the cycle-steal clock at X7, block clock advance must be at the CPU terminator no sooner than X4 and no later than the leading edge of X7.

No cycle-steal device may be overlapped if the X-clock is blocked at X2. Only the resident disk storage drive may be overlapped if the X-clock is blocked at X7.

A SAC cycle-steal automatically blocks lower level cycle-steal operations for the duration of the SAC cycle-steal.

Channel Cycle-Steal Request: This line is used by SAC to initiate a cycle-steal operation.

SAC I Attachment: The cycle-steal priority is set in the CPU at T7-X7-phase B time. To insure the next cycle is a cycle-steal, this request must be at the CPU terminator no later than the leading edge of T7 or X7. This request should be turned off no later than X6 time of the cycle which is honoring it in order to avoid a second request and to avoid getting two consecutive cycles.

SAC II Attachment: To insure that the next cycle is a cycle-steal, this request must be at the 1133 terminator no later than the trailing edge of T4 or X4. Once activated, this request must not be dropped during the following time interval: from the trailing edge of T4 or X4 to the trailing edge of T7 or X7. The request must be turned off no later than the trailing edge of X4 time. If taking more than one cycle, do not drop this line.

Channel Address In: This bus gates in the core storage address for a cycle-steal operation. The channel address is gated by cycle-steal level 1 at the CPU. The address must be stable at the CPU terminators from the leading edge of X0 through X6. The IBM devices on the 1133 increment the cycle-steal address at the fall of X6 on a 3.6-microsecond system or X6 and phase B on a 2.2-microsecond system.

The cycle-steal address is normally presented with the cycle-steal request and maintained thru X6.

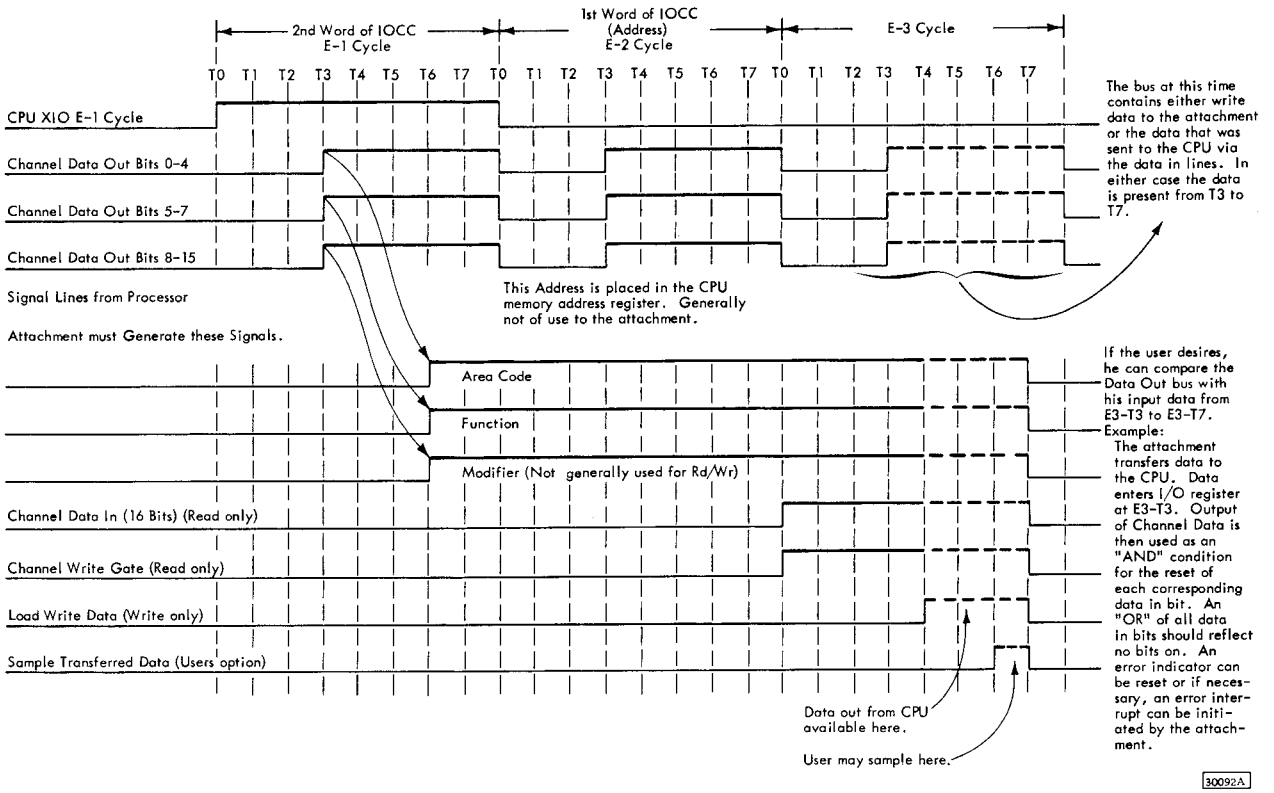


Figure 9. SAC I/O Timing Diagram - XIO Read or Write

For continuous cycle-steals, the address is normally changed after X6 and before X0 of the following cycle. With the additional delays for an OEM device on SAC II, this timing could be critical. For this reason, an additional address register is provided in the 1133 for the OEM user on SAC II. This register holds the contents of the address in lines, from SAC II, from X2 through X6. The OEM user's device can then change the OEM device address any time between X2 and the start of X6.

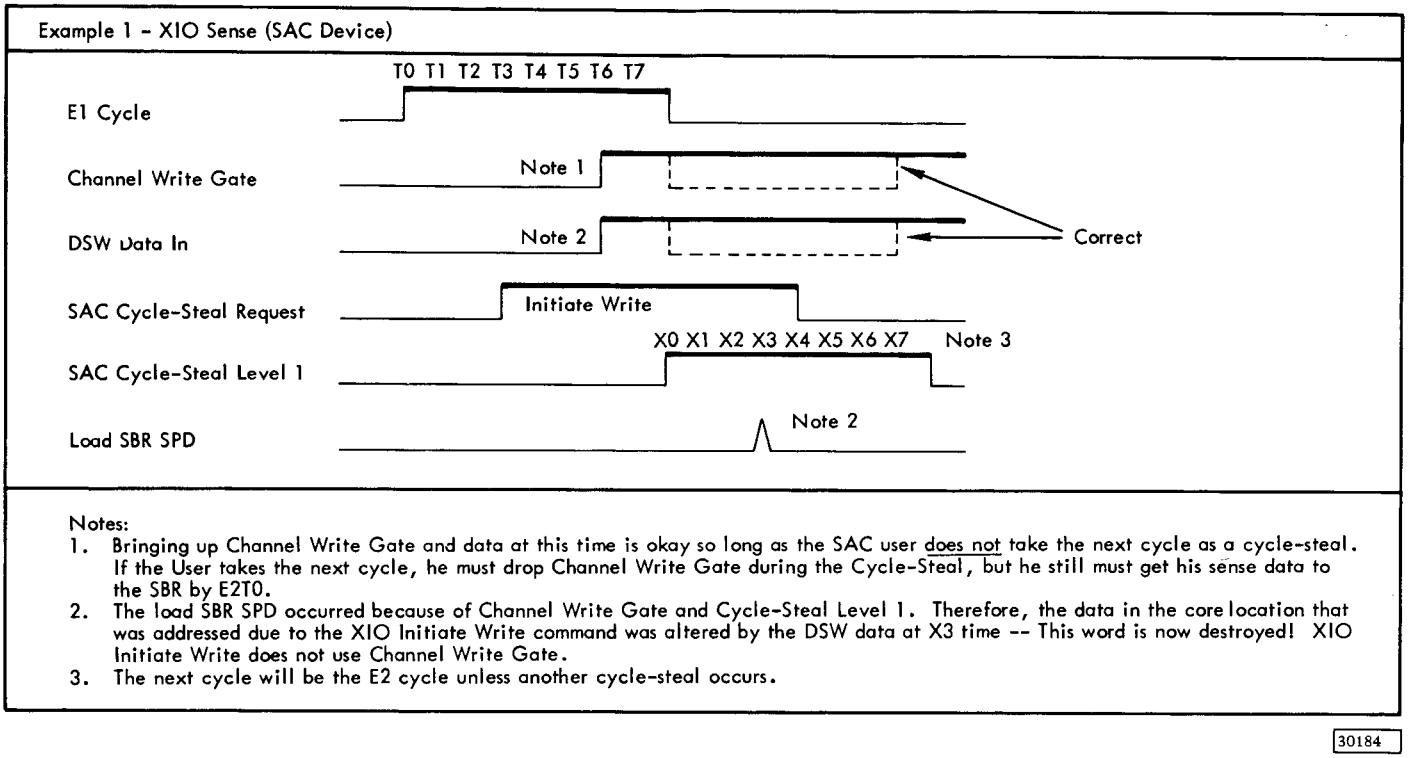
CPU Meter Out: This signal indicates that the CPU meter is running. It is used to condition the operation of the usage meters of external devices.

CPU Meter In: This line indicates that a device is completing its operation after receiving a CPU instruction. It is used to condition the CPU usage meter for operation in accordance with IBM usage metering policy.

CPU Clock Out: This signal indicates that the CPU clock is running (T- or X-clock). It is used to gate the enable/disable switches on the system. Before any device can change status (e.g., enable or disable) this signal must not be active.

CPU Parity Stop: This signal indicates that the CPU has detected a parity error and halted.

Inhibit Cycle-Steal Request: This line should be used by the OEM device to inhibit the channel cycle-steal request in instances where the percentage of CPU cycles used by the SAC device is such that lower priority devices may be pre-empted enough to cause loss of data.



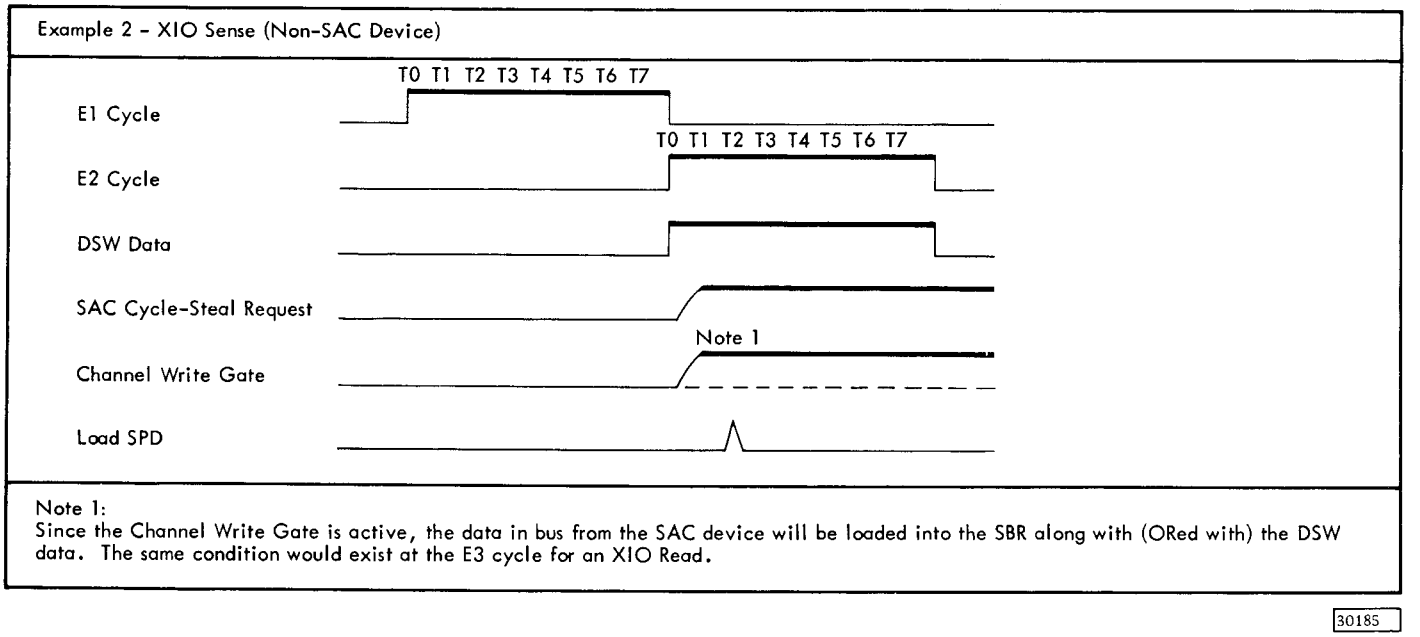


Figure 12. Examples of a SAC Device Destroying Data by Improper Control of the Channel Write Gate

Line Drivers and Terminators for SAC

The SAC signal line driver and terminator circuits are shown in Figures 13 and 14.

When the IBM 1133 is attached to these lines, the circuits operate within the "normal" level. However, the circuits will operate efficiently outside of this normal level as long as the maximum levels are not exceeded.

> Note: The maximum levels shown are absolute, which means that noise must not go beyond these limits. Since it is not possible to completely eliminate noise, the OEM user should try to operate at the normal level.

The signal lines to and from these circuits are connected to a 160-pin connector. Each line is made up of a pair of twisted wires. One of the wires in each pair is intended to be a grounded shield and should be tied to ground at both ends.

Power Sequence for SAC Devices

I/O devices attached to the SAC should not be turned on or off while the CPU is processing. To power down a device, the CPU should either be off or in single step mode. To power a device, the CPU should also be either off or in single step mode.

Cabling to OEM Device

The recommended bulk cable for attachment of an OEM device to the storage access channel is IBM part 2158929. (A cable with connectors is available from IBM as part 2243004. See IBM 1130 Installation Manual - Physical Planning (Form A26-5914). Characteristics of the recommended bulk cable are:

Number of conductors = 182 (91 twisted pair)
Cable diameter = 1.16" - 1.24"
Cover type = Polyvinyl chloride 5/64" thick
One twist every 1" ±0.12"
Shielding = Tinned copper braid for 90% minimum coverage
Cable Lay-up = 1-6-12-18-24-30
Individual Conductor Characteristics:
- Quantity = 182 (91 twisted pair)
- Maximum outside diameter = 0.054"
- AWG size = 22
- Conductor material = stranded copper
- Insulation material = semi-rigid polyvinyl chloride
- Insulation thickness = 0.009" nominal
- U. L. voltage rating = 300 volts
- Temp. rating (insulation) = 80°C, 176°F
- Nominal delay = 2.3 nanoseconds/foot

The external shielding must be connected only to CPU ground through position L3 of the 160-pin receptacle for the SAC.

OEM Attachment

Data, address, and control lines are brought out through a 160-pin receptacle located in the I/O entry area at the rear of the 1131.

The mating plug for quick-disconnect attachment to the 1131 CPU is shown in Figure 15.

Coupled Noise

The maximum level for noise coupled onto any signal line must not exceed 300 millivolts.

Cable Resistance

Cable length is limited by cable resistance and contact resistance. The maximum cable resistance, including contact resistance, must not exceed 26 ohms.

SAC Power Sequence			
1131 to SAC I or 1133		1133 to SAC II	
Line Title	Connector Position	Line Title	Connector Position
Convenience AC	PC5-17		
Convenience Common	PC5-18		
SAC Shield Ground	PC5-19		
Emergency Power Off Switch	PC5-21	SAC II Emergency Power Off Switch	CC5-23**
Emergency Power Off Switch	PC5-26	SAC II Emergency Power Off Switch	CC5-28**
SAC Sequence 24 Vac	PC5-22	SAC II Sequence 24 Vac	CC5-22
SAC Sequence 24 Vac Com.	PC5-27	SAC II Sequence 24 Vac Com.	CC5-27
SAC Emergency Power Off	PC5-23*	SAC II Emergency Power Off	CC5-21
SAC Emergency Power Off	PC5-28*	SAC II Emergency Power Off	CC5-26

* If SAC device is not using PC5, then jumper PC5-23 to PC5-28.

** If SAC II device is not using CC5, then jumper CC5-23 to CC5-28.

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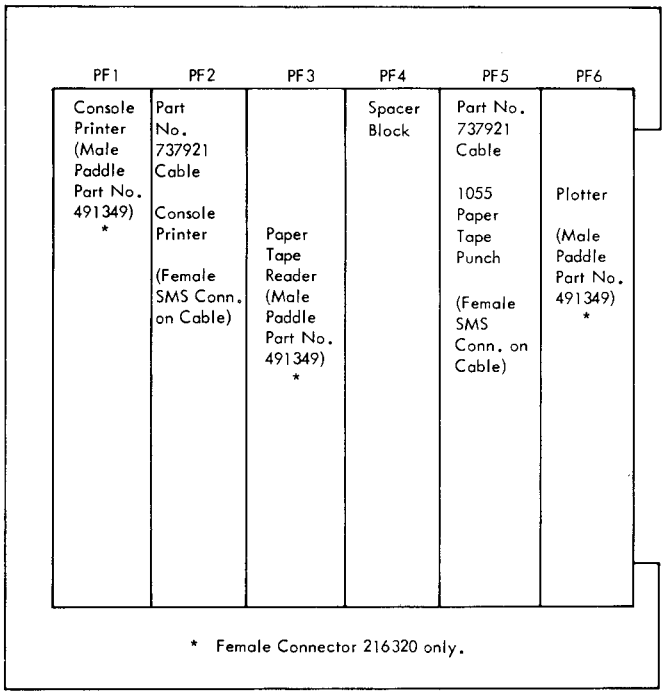
Figure 32. SAC Sequence Power Connections



I/O Signal Feed Through Panel (PF) View from CPU-SMS Paddle Card Side.

BR0057

Figure 33. I/O Signal Panel

Connection	Line Title	Connection	Plug P5
-	PF6A to 6F No Connection	-	-
A-C1N5B10	-24v Ready	PF6G	16
-	--	PF6H	N.C.
-	No Connection	PF6J	-
-	No Connection	PF6K	-
A-C1N5D05	-Pen Down Drive	PF6L	12
A-C1N5B04	-Pen Up Drive	PF6M	11
A-C1N5D04	-Carr Left Drive	PF6N	7
A-C1N5B03	-Carr Right Drive	PF6P	8
A-C1N5D02	-Drum Down Drive	PF6Q	6
A-C1N5B02	-Drum Up Drive	PF6R	5

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Figure 34. 1627 Plotter Signal Connections

Connection	Line Title	Connection
A-C1A4B02	-Select T2	PF1A
A-C1A4D02	-Select T1	PF1B
A-C1A4B03	-Select R2A	PF1C
A-C1A4D04	-Select R1	PF1D
A-C1A4B04	-Select R5	PF1E
A-C1A4D05	-Select R2	PF1F
A-C1A4B05	-Select Aux	PF1G
A-C1A4D06	-Line Feed	PF1H
A-C1A4B07	-Tab	PF1J
A-C1A4D07	-Cr-Lf and EOL	PF1K
A-C1A4B08	-Up Shift	PF1L
-	No Connection	PF1M
-	No Connection	PF1N
-	No Connection	PF1P
-	No Connection	PF1Q
A-C1A4D09	-Down Shift	PF1R
PF2A	+Twr End Of Line	A-C1A4B09
PF2B	No Connection	-
PF2C	+12v E.O.L. Input	PF2L
PF2D	No Connection	-
PF2E	-Twr CB Response	A-C1A4D10
PF2F	Car Ret Inlk	Not Used
PF2G	Crlft Inlk 2	Not Used
A-C1A4B10	-Space	PF2H
A-C1A4D11	-Backspace	PF2J
A-C1A4B12	-Black Ribbon Shift	PF2K
PF2L	-Twr End Of Forms	A-C1A4D12
PF2M	No Connection	-
PF2N	+Twr Crlft Inlk	A-C1A4B13
A-C1A4D13	-Red Ribbon Shift	PF2P
Not Used	Double Line Feed	PF2Q
Not Used	Single Line Feed	PF2R

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Figure 35. 1131 Console Printer Connections

Connection	Line Title	Connection
PF5A	Backspace Punch	Not Used
-	R & S Counter	PF5B
PF5C	No Connection	-
PF5D	No Connection	-
PF5E	No Connection	-
A-B1N5D04	-Drive P.T. Punch Clutch	PF5F
A-B1N5B08	-P.T. Punch 8th Chan Drive	PF5G
PF5H	-P.T. Punch Ready	A-B1N5B03
PF5J	GND 8th Chan	Not Used
A-B1N5B09	-P.T. Punch C Drive	PF5K
A-B1N5D06	-P.T. Punch 1 Drive	PF5L
A-B1N5B10	-P.T. Punch 2 Drive	PF5M
A-B1N5D10	-P.T. Punch 4 Drive	PF5N
A-B1N5B13	-P.T. Punch 8 Drive	PF5P
A-B1N5D07	-P.T. Punch A Drive	PF5Q
A-B1N5B07	-P.T. Punch B Drive	PF5R

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Figure 36. 1055 Paper Tape Punch Signal Connections

Connection	Line Title	Connection
A-B1A6D02	-P.T. Rdr. Clutch Drive B	PF3A
Not Used	Reverse Drive A	PF3D
Not Used	Reverse Drive B	PF3E
A-B1A6D06	-P.T. Rdr. Clutch Drive A	PF3F
-	No Connection	PF3G
-	No Connection	PF3H
PF3K	-P.T. Read Contact C	A-B1A6B10
PF3L	-P.T. Read Contact 1	A-B1A6B04
PF3M	-P.T. Read Contact 2	A-B1A6B05
PF3N	-P.T. Read Contact 4	A-B1A6D07
PF3P	-P.T. Read Contact 8	A-B1A6D09
PF3Q	-P.T. Read Contact A	A-B1A6D13
PF3R	-P.T. Read Contact B	A-B1A6D12
PF3C	-P.T. Read Contact 8th CH	A-B1A6B12
PF3B	-P.T. Reader Ready	A-B1A6B03

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Figure 37. 1134 Paper Tape Reader Signal Connections